to-ground (represented by the capacitors shown in phantom in FIG. 1 and designated C_{S1} and C_{S2}) is coupled to opposite plates of capacitor Cx. Capacitor C_{S1} is charged to V_{REF} and discharged to ground through buffer amplifier **8** during each period of the clock signal **CK1**. The charge on capacitor C_{S1} does not contribute to the charge on capacitor Cx or to the currents at the summing junction **14** of operational amplifier **16** and, therefore, there is no contribution to output voltage V_{OUT} from capacitor C_{S1}. Capacitor C_{S2} also does not contributute to the charge on capacitor Cx or to the current at summing junction **14**, since capacitor C_{S2} is shunted by the on-resistance of JFET **12** when capacitor Cx is being charged to V_{REF}. Therefore, capacitor C_{S2} accumulates no net charge during the charging cycle of capacitor Cx.

By virute of the present invention, a relatively simple, low power, low cost capacitance-to-voltage converter is provided which minimizes the effects of stray capacitance-to-ground and clock feedthrough on the accuracy of measuring an unknown capacitance of a capacitor under measurement. Moreover, the converter also allows a highly accurate determination of such capacitance when the capacitor under measurement is remotely connected to the circuit by shielded cables. The present capacitance-to-voltage converter completely eliminates the problems associated with conventional switched capacitor converters, because clock feedthrough and stray capacitance-to-ground have virtually no effect on the accuracy of the capacitance measurement. What is more, by using miniature shielded probes, the present capacitance-to-voltage converter is also suitable for accurately measuring small value capacitors (e.g. integrated MOS capacitors and hybrid circuit chip capacitors), because of its inherent ability to virtually eliminate error from stray capacitance-to-ground sources. More specifically, test results performed on the disclosed converter show that the voltage V_{OUT} at the output terminal **17** of operational amplifier **16** tracks the capacitance of capacitor Cx to within the ± 0.01 picofarard or $\pm 0.05\%$ full scale for a 20 picofarad full scale output.

It will be apparent that while a preferred embodiment of the invention has been shown and described, various modifications and changes may be made without departing from the true spirit and scope of the invention. For example, equivalent devices could be substituted for the switching devices illustrated in FIG. 1 for implementing circuit **1**. More particularly, n-channel field effect transistors could be substituted for JFETs **10** and **12**, if the polarity of V_{REF} and all clock signals were to be reversed. Moreover, MOSFETs could also be used in place of JFETs **10** and **12**. In addition, changes to the timing of clock signals Ck1, CK2 and Ck3 may be made, for example, to simplify the design of the clock generator **6** or, for example, to accommodate large capacitance ratios of Cx to C_{S2}. When the ratio of Cx to C_{S2} is large, the potential across C_{S2} momentarily approaches V_{REF} at a time when Ck1 goes relatively high and before Ck2 goes relatively low. This potential may cause JFET **10** to beocme conductive which will introduce a nonlinearity into V_{OUT}. To prevent this momentary potential buildup on C_{S2}, the clock generator **6** can be modified to have the rising edge of CK1 coincide with the falling edge of Ck2 which causes JFET **12** to become conductive as CK1 goes relatively high, whereby to shunt any charge buildup on C_{S2} to ground.

Extensions of the present invention could include using V_{REF} as the reference voltage for a digital voltmeter instrument or integrated circuit to ratiometrically measure the output voltage V_{OUT} to thereby remove variations in V_{REF} from V_{OUT}.

Having thus set forth a preferred embodiment of the present invention, what is claimed is:

1. A circuit for providing an accurate measurement of the capacitance of a capacitor, said circuit comprising:

clock signal generator means for providing a signal which alternates between relatively high and low signal levels, said signal generator means interconnected with a first plate of said capacitor to supply said clock signal thereto;

operatonal amplifier means having first input terminal means connected to a summing node, second input terminal measn connected to ground, and output terminal means providing an output voltage signal, said capacitor being discharged into said summing node at the first input terminal means of said operational amplifier means; and

means for successively charging and discharging said capacitor as said clock signal alternates between relatively high and low signal levels, said charging and discharging means including switch means connected between the second plate of said capacitor and said summing node;

the magnitude of the voltage signal at the output terminal means of said operational amplifier means providing a measurement of the capacitance of said capacitor.

2. The circuit recited in claim **1**, wherein said means for charging and discharging said capacitor also includes a buffer amplifier connected between said clock signal generator means to receive said clock signal therefrom and the first plate of said capacitor for charging said capacitor each time that said clock signal is at the relatively high signal level, the closure of said switch means discharging said capacitor into said summing node each time that said clock signal is at the relatively low signal level.

3. The circuit recited in claim **1**, further comprising a charge catching capacitor connected to the first input terminal means of said operational amplifier means to reduce the amplitude of switch transients from said switch means and thereby prevent the saturation of said operational amplifier means.

4. The circuit recited in claim **1**, wherein said switch means includes at least one multi-terminal semiconductor device having a conduction path connected between the second plate of said capacitor and said summing node at the first input terminal means of said operational amplifier means.

5. The circuit recited in claim **4**, wherein said multiterminal semiconductor device is a field effect transistor having a pair of conduction path terminals and a control terminal.

6. The circuit recited in claim **5**, wherein said switch means comprises a pair of said field effect transistors having their respective conduction paths connected in electrical series between the first input terminal means of said operational amplifier means and ground.

7. The circuit recited in claim **6**, wherein said clock signal generator means is connected to the respective control terminals of said pair of field effect transistors to control the operations thereof.